VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (CURRENTLY AMENDED) An apparatus comprising:

a first look-up-table [one or more look-up-tables (LUTs)] configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal; [provide logical functions]

a second look-up-table configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal; and

a logic circuit configured to generate an output signal in response to said first partial product signal and said second partial product signal, wherein said [one or more LUTs] first look-up-table and said second look-up-table are implemented within a multiport memory.

5. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein [each of] said first input signal [one or more LUTs] is substantially equal to one of said third input signal and said fourth input signal [configured to receive one or more inputs].

6. (CURRENTLY AMENDED) The apparatus according to claim [5] 1, wherein [each of] said first input signal [one or more

inputs comprise] comprises a single-bit [or multi-bit input in a] serial [or parallel] configuration.

7. (CURRENTLY AMENDED) The apparatus according to claim [5] 1, [wherein each of said one or more LUTs is] further comprising:

a third look-up table configured to generate a third partial product signal from a third address formed by concatenating said first input signal and said fourth input signal.

8. (CURRENTLY AMENDED) The apparatus according to claim [8] 7, [wherein each of said one or more LUTs is] further comprising:

a fourth look-up-table configured to [present said] generate a fourth partial product signal [in response to] from a fourth address formed by concatenating said [one or more inputs] second input signal and said third input signal.

9. (CURRENTLY AMENDED) The apparatus according to claim 8, [further comprising] wherein said logic [adder] circuit is further configured to [receive said one or more partial product signals and present an] generate said output signal in further response to said third partial product signal and said fourth partial product signal.

10. (CURRENTLY AMENDED) The apparatus according to claim [9] 1, wherein said [adder] logic circuit is further configured to shift said first partial product signal in response to a first shift signal before generating [present] said output signal [in response to one or more second signals].

11. (CURRENTLY AMENDED) The apparatus according to claim 10, wherein said logic circuit is further [comprising a routable interconnect] configured to shift said second partial product signal in response to a second shift signal before generating said output signal.

12. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising:

[one or more register configured to increase a throughput of] a plurality of registers disposed between said [one or more] first and said second look-up-tables and said logic circuit.

13. (CURRENTLY AMENDED)The apparatus according to claim 1, wherein said first partial result signal is an [logical functions comprise] arithmetic function of said first input signal and said second input signal [functions and other logic functions].

14. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a first partial product signal by [providing one or more look-up-table (LUTs)] looking-up a first address formed by concatenating a first input signal and a second input signal to [in] a multiport memory;

means for generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

means generating an output signal in response to said first partial product signal and said second partial product signal [for providing one or more logical functions, in response to said one or more LUTs, to at least one port of said multiport memory].

15. (CURRENTLY AMENDED) A method for implementing logical functions, comprising the steps of:

(A) generating a first partial product signal by [providing one or more look-up-tables (LUTs)] looking-up an address formed by concatenating a first input signal and a second input signal to [in] a multiport memory;

(B) generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

(C) [(B)] generating an output signal in response to said first partial product signal and said second partial product signal

[providing one or more logical functions, in response to said one or more LUTs, to at least one port of said multiport memory].

16. (CURRENTLY AMENDED) The method according to claim [14] 15, wherein said first partial product signal is a logical function of said first input signal and said second input signal [multiport memory comprises a dual port or quad port memory].

17. (CURRENTLY AMENDED) The method according to claim [14] 15, [further comprising:] wherein said first input signal has [receiving one or more input signals, each comprising] a single-bit [or multi-bit input in a] serial [or parallel] configuration.

18. (CURRENTLY AMENDED) The method according to claim [14] 15, wherein said multiport memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, a flash memory and other appropriate types of memory.

19. (CURRENTLY AMENDED) The method according to claim [14] 15, [further comprising] wherein step (C) comprises the [steps] step of:

[(C) presenting one or more] adding said first partial product [signals; and] signal and

[(D) adding] said second [one or more] partial product signal [signals].

20. (CURRENTLY AMENDED) The method according to claim [14] 19, [wherein step (D)] further comprising the step of:

shifting said first partial product signal [is further configured] in response to [one or more] a first shift [signals] signal before adding to said second partial product signal.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first look-up-table, a second look-up-table and a logic circuit. The first look-up-table may be configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. The second look-up-table may be configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal. The logic circuit may be configure to generate an output signal in response to the first partial product signal and the second partial product signal. The first look-up-table and the second look-up-table may be implemented within a multiport memory

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 5 lines 12-21, page 7 lines 1-9, page 11, lines 16-18 and FIGS. 1-2, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 8-11 and 14-20 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn..

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-11 and 13-20 under 35 U.S.C. §102(b) as being anticipated by White '151 has been obviated by appropriate amendment and should be withdrawn.

White discloses a ROM-based complex multiplier useful for FFT butterfly arithmetic unit (Title). White does not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. In contrast, White appears to be silent for each memory 21-28 utilizing an address formed by concatenating **two input signal**. Therefore, White does not appear to disclose or suggest a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal as presently claimed. Claims 14 and 15 use language similar to claim 1. As such, the claimed invention is

fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore claims 1, 14 and 15 provides a multiport memory. Claim 2 provides a dual port memory. Claim 3 provides a quad port memory. In contrast, White appears to be silent regarding dual, quad or multiport memories. White does mention that the digital complex multiplier has four ports. However, each memory element 21-28 in FIGS. 1-6 of White appear to be **a single-port memory.** Therefore, White does not appear to disclose or suggest a dual port memory, a quad port memory or a multiport memory as presently claimed. As such, claims 1, 2, 3, 14 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides a first input signal that is substantially equal to one of a third input signal and a fourth input signal. In contrast, White appears to be silent regarding using a substantially equal signal for two addresses into two of the memory elements 21-28. In particular, FIGS. 1-6 appear to disclose that the address received by each memory element 21-28 is unique. Therefore, White does not appear to disclose or suggest a first input signal that is substantially equal to one of a third input signal and a fourth input signal as presently claimed. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a first input signal that comprises a single-bit serial configuration. In contrast, FIGS. 7-9 of White appear to disclose that the four input signals have a multi-bit parallel configuration. The rest of White appears to be silent regarding a single-bit serial configuration. Therefore, White does not appear to disclose or suggest a first input signal that comprises a single-bit serial configuration as presently claimed. Claim 17 provides language similar to claim 6. As such, claims 6 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 7 provides a third look-up table configured to generate a third partial product signal from a third address formed by linking the first input signal and the fourth input signal. Claim 8 provides a fourth look-up-table configured to generate a fourth partial product signal from a fourth address formed by linking the second input signal and the third input signal. In contrast, White appears to be silent for using the same input signal at two memory elements 21-28. In particular, each memory element 21-28 in FIGS. 1-6 of White appears to have a unique input signal. Therefore, White does not appear to disclose or suggest a third look-up table configured to generate a third partial product signal from a third address formed by linking the first input signal and the fourth input signal or a fourth look-up-table configured to generate a fourth partial product signal from a

fourth address formed by linking the second input signal and the third input signal as presently claimed. As such, claims 7 and 8 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over White in view of Chehrazi et al. '843 has been obviated by appropriate amendment and should be withdrawn.

Claim 12 depends directly from independent claim 1 which is now believed to be allowable. As such, claim 12 is also fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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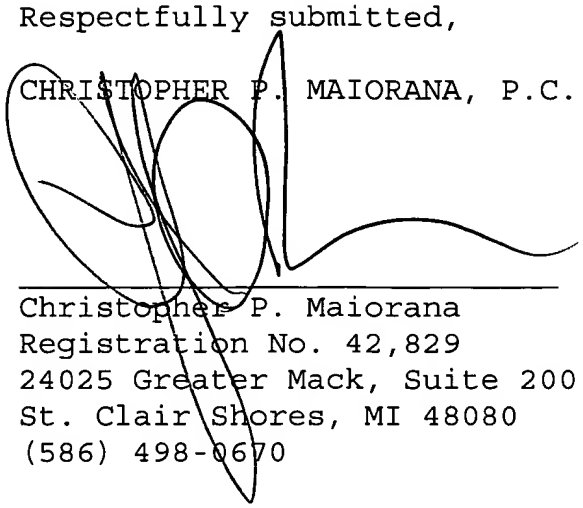

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